VHDL LANGUAGE AND DESIGN FLOW

14 May - 18 May 2018

WHY PARTICIPATE
The increasing complexity of digital circuits brings about the need for a design methodology that allows a short design cycle, while maintaining architectural flexibility, re-use of IP blocks and easy documentation. VHDL is a standard worldwide language for the design, documentation and description of electronic systems on the component, board or system level. It supports design verification through simulation and design creation through synthesis. Simulation and synthesis are however not the only tools used in the design flow of an ASIC. Digital frontend designers nowadays also have need of knowledge about a whole set of tools such as static timing analysis, test insertion, power analysis and test pattern generation. This 5-day course 'VHDL language and design flow' is centered on VHDL syntax (through example) while emphasizing good code style and the link to hardware. During the course the participants will:

• Be introduced to VHDL and the test-bench concepts.
• Learn how to efficiently simulate VHDL models.
• Be introduced to the VHDL synthesizable sub-set.
• Learn that ‘what you write is what you get’, i.e. that the synthesized netlist is dependent on how the code is written.
• Learn how to tackle issues like: sharing, asynchronous logic, initialization.
• Get some experience with synthesis of the VHDL code into a gate level netlist using clock gating techniques to reduce the power.
• Learn how to insert basic test logic and generate test patterns.
• Be introduced to performing power analysis, generating test patterns and running logic equivalence checks.

WHO SHOULD ATTEND
This course focuses on (junior) system design engineers targeting FPGA and ASIC.

WHY IMEC ACADEMY
Imec academy acts as the learning lever for both imec own employees and the local and international industry and academia. We strive to educate, develop and inspire individuals and groups to empower them to stay successful in their research and development: learning for excellence.

Our unique high-tech environment and our international top-talent enable us to combine advanced world-class expertise with hands-on applications in the domains in which imec excels.

LECTURING TEAM
Roeland Vandebriel, Steven Dupont, Jorgo Tsouhlarakis and Fraderic Joseph.
INTRODUCTION
• Complete flow overview: from specification to tested dies
• VHDL background, versions & basics concepts
• Entities, architectures, process, hierarchy
• Labs
• Tools used: Modelsim for simulation

ROELAND VANDEBRIEL

VHDL FOR SYNTHESIS
• Packages, libraries, types, signals, variables
• Logic and memory inference
• High level optimizations (resource sharing etc.)
• Labs
• Tools used: Synopsys Design Compiler

ROELAND VANDEBRIEL

VHDL TESTBENCHES (VHDL 2008)
• Functions, procedures, records, file IO
• Self checking / self stopping
• Coverage
• Labs
• Tools used: Modelsim

STEVEN DUPONT

INTRODUCTION TO LOGIC SYNTHESIS
• Logic synthesis design flow basics with DC compiler of Synopsys
• Timing constraints
• Optimisation control
• Datapath synthesis
• Clock gate insertion
• Scan insertion
• Labs
• Tools used: Synopsys Design Compiler

JORGO TSOUHLARAKIS
FINAL STEPS BEFORE TRANSFERRING THE NETLIST TO THE LAYOUT TEAM

- ATPG
- Power analysis
- Formal verification
- Labs
- Tools used: Synopsys TetraMax for ATPG, Synopsys Primetime for Power analysis, Cadence Formality for Formal verification

FRADARIC JOSEPH
PROGRAM OVERVIEW

VHDL LANGUAGE
AND DESIGN FLOW

MON 14.05.18
09.00 - 17.00
Introduction

TUE 15.05.18
09.00 - 17.00
VHDL for synthesis

WED 16.05.18
09.00 - 17.00
VHDL testbenches (VHDL 2008)

THU 17.05.18
09.00 - 17.00
Introduction to logic synthesis

FRI 18.05.18
09.00 - 17.00
Final steps before transferring the netlist to the layout team